REMARKS

This communication responds to the Office Action mailed on July 6, 2005. Claims 17, 20, 24, and 26 are amended, no claims are canceled, and no claims are added. As a result, claims 1-26 are now pending in this Application.

§*101 Rejection of the Claims*

Claims 24-26 were rejected under 35 USC § 101 because the claimed invention is directed to non-statutory subject matter. Claim 24 has been amended so as to be directed to a "computer-readable" medium having associated data, wherein the data, when accessed, results in a "computer" performing various activities. Claim 26 has been amended to conform to the textual amendments made to claim 24. The amendments to claims 24 and 26 have been made in the interests of temporal economy, so as not to unduly prolong the interpretive disagreement between the Examiner and the Applicant, and not for reasons related to patentability. The concerns of the Examiner should now be addressed, and the Applicant therefore respectfully requests the rejection of these claims be reconsidered and withdrawn.

§*102 Rejection of the Claims*

Claims 5-16 and 24-26 were rejected under 35 USC § 102(b) as being anticipated by Bowers (U.S. 6,308,285 B1). Claims 18 and 19 were rejected under 35 USC § 102(e) as being anticipated by Falik et al. (U.S. 6,065,078). First, the Applicant does not admit that Bowers or Falik are prior art, and reserve the right to swear behind these references in the future. Second, since neither Bowers nor Falik anticipate each and every element of the invention as claimed by the Applicant, these rejections under 35 U.S.C. § 102 are respectfully traversed.

As admitted in the Office action, the sleep signal SLP# of Bowers is "delivered to *each* processor" such that "all processors are placed into a sleep mode." *See* Office Action, Mail Date 20050128, pg. 4, lines 6-8 and Bowers, Col. 2, line 53. This method of operation

by Bowers is further supported by the Office Action admission that "The processors also stop executing commands ...". Office Action, pg. 4, line 10. That is, Bowers uses a controller (programmable array logic) to put each and every processor in the system to sleep, which is necessary, because this operation permits any one of the processors in Bowers to be physically replaced. *See* Bowers, Col. 2, lines 53-56. As a matter of contrast, in the embodiments claimed by the Applicant, one processor taken from the plurality of processors (e.g., the monarch processor) remains awake while other processors are put to sleep.

Given the method of operation disclosed in Bowers, the Office Action rejects the instant claims by attempting to characterize Bowers' controller as a "monarch processor." However, this is inappropriate. First, because Bowers makes a clear distinction between the "controller" and the "processors." It is *only* the controller in Bowers, and not the processors, that can access data used to put the processors to sleep. Second, even if one accepts the premise that Bowers' controller can operate as a monarch processor, the conclusion would be that Bowers' controller, as one of the plurality of processors, could also be put to sleep for replacement as directed by one of the other processors in Bowers' system. This type of operation, claimed by the Applicant, is not possible using Bowers' system.

Therefore, Bowers does not teach or suggest a "monarch processor being capable of executing the error handling routine to correct the error ..." as claimed by the Applicant in independent claim 5 (and dependent claims 6-7) such that "the monarch processor is capable of sending a wake up signal to the plurality of slave processors to exit the rendezvous state" as claimed in claim 7.

Further, Bowers does not teach or suggest "a plurality of processors including a monarch processor ... and an interrupt signaling mechanism ... to initiate a rendezvous state ... being a state where all of the plurality of processors but the monarch processor are idle" as claimed by the Applicant in independent claim 8 (and dependent claims 9-11). In addition, Bowers does not teach or suggest "a plurality of processors ... and an operating system layer ... to signal all but one of the plurality of processors to end a rendezvous state ... upon receiving a signal that error handling is completed, said rendezvous state being a

state wherein all but the one of said plurality of processors are idle" as claimed by the Applicant in independent claim 12 (and dependent claims 13-15).

Bowers also does not teach or suggest "detecting an error ...; entering a rendezvous state in which all processors but the one processor included in the multiple processor system are idle; ... and ... correcting the error using the one processor" as claimed by the Applicant in independent claim 15 (and dependent claims 16-17). Finally, Bowers does not teach or suggest "attempting to correct an error ... in a multiple processor system ... and on failure, entering a rendezvous state to correct the error, said rendezvous state being a state where all but one of the processors included in the multiple processor system are idle" as claimed by the Applicant in claim 24 (and dependent claims 25-26).

Falik suffers from similar deficiencies. Specifically, Falik fails to disclose "attempting to correct an error by a detecting processor included in a multiple processor system" and "entering a rendezvous state to correct the error, said rendezvous state being a state where all but one of the processors included in the multiple processor system are idle" as claimed in claims 18 and 19. While the Office Action asserts that Falik's debugger interface is somehow equivalent to a "detecting processor included in a multiple processor system", this does not comport with the clear distinction Falik makes between the host computer 1820 and the multiprocessor integrated circuit 1810. *See* Falik, Col. 2, lines 37-40 and FIG. 18. Even if it is assumed that Falik's debugger can operate as a "detecting processor", how does Falik's system correct the error? Falik's debugger, or a monitor, are the only resources available, and neither one operates to "correct" the error. It is respectfully noted that the term "error" appears only once in Falik, concerning bus communication error probability. However, such errors are not processed by Falik's system. *See* Falik, Col. 18, lines 31-32. In fact, Falik states that, while such errors can be cured by a system reset, such operation should be "avoided by the host" since this resets the entire chip. *See* Falik, Col. 18, lines 39-47.

The Applicant agrees that the term debug, by definition, may include correcting logical or syntactical errors. However, there mere fact that debugging activity occurs does not disclose the agency by which the actions are accomplished. For example, debugging

typically occurs using human decision processes to propose and test solutions. This is not the same as what is claimed by the Applicant, where the a detecting processor itself can operate by "attempting to correct an error ...". This type of activity is not disclosed by Falik.

Finally, how can "all but one of the processors included in the multiple processor system" be idle, as asserted in the Office Action, if at least one processor in the multiprocessor integrated circuit 1810 must be awake to execute a monitor, *in addition* to the processor running the debugger on Falik's host computer? The debugger communicates with the monitor on one of the processors, which means at least *two* processors must be operational to debug programs in Falik's system. See Falik, Col. 17, lines 27-46. This is not what is claimed by the Applicant.

In short, what is disclosed by Bowers and Falik is not identical to what is claimed by the Applicant, and therefore, the rejection under § 102 is improper. Reconsideration and allowance of claims 5-16, 18-19, and 24-26 is respectfully requested.

§103 Rejection of the Claims

Claim 17 was rejected under 35 USC § 103(a) as being unpatentable over Bowers and further in view of Fujii et al. (U.S. 5,892,898). Claim 17 has been amended to clarify that a severe error is one where the detecting processor is unable to handle the error except by terminating a process, as stated in the Application. *See* Application, pg. 7, line 1 – pg. 8, line 3. No new matter has been added. The amendment to claim 17 has been made in the interests of temporal economy, so as not to unduly prolong the interpretive disagreement between the Examiner and the Applicant, and not for reasons related to patentability. The concerns of the Examiner should now be addressed, and the Applicant therefore respectfully requests the rejection of this claim be reconsidered and withdrawn.

Allowable Subject Matter

Claim 20 was objected to as being dependent upon a rejected base claim, but was indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claim 20 has been amended herein to include the

intervening limitations of claims 18 and 19, and not for reasons related to patentability. Thus, claim 20 should be in condition for allowance. The Applicant notes with appreciation that claims 1-4 and 21-23 have been allowed.

CONCLUSION

The Applicant respectfully submits that all of the pending claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone the Applicant's attorney, Mark Muller at (210) 308-5677, or Applicant's below-named representative to facilitate the prosecution of this Application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

SURESH MARISETTY ET AL.

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 31 day of August 2005.

Name Signature